Please substitute amended claim 37 for pending claim 37 as follows:

37. (Amended) The method of **claim 31**, further comprising the step of providing in the chip area a ridge defined on the main surface between the photosite and the groove.

REMARKS

In the most recent Office Action, the Drawings were objected to for including a reference numeral which was not referenced in the Specification. In the above amendment, the Specification has been amended to reference the reference number 12. No change to the Drawings is deemed necessary in view of the Amendment to the Specification.

In the Office Action, claims 4 and 5 are objected to as being in improper dependent form. Claims 4 and 5 have been cancelled.

In the Office Action, claim 31 is objected to as being in improper dependent form. The claim has been corrected as per the Examiner's suggestion.

Claims 1-37 have been rejected under 35 USC 103 as being unpatentable over Hosier '019 in view of Lin '730.

Of the claims under rejection, claims 1, 11, 20, and 31 are independent. Although the various claims are directed to, respectively, a chip, an apparatus having a chip, a wafer (from which chips can subsequently be diced), and a method of making a chip, at least one essential feature is common to all of the independent claims: the chip, however made, includes a portion of a **groove** which defines an ***edge*** of the chip. A light-transmissive planar layer extends **over** this groove, or in effect over the edge of the chip.

An embodiment of this claimed feature is shown in the specification as filed at Figure 3 (for a chip which has not yet been diced from a wafer) or at Figure 5 (for chips which have been diced and installed in a larger apparatus).

Each chip 10 defines an edge having a portion of a groove 70. Although the side of the groove 70 slants downward from the main (top) surface of a chip 10, because the planar layer 72 extends over the portion of the groove 70, the overall top surface of the chip 10 is made planar even over the grooves 70.

The practical advantage provided by this chip and wafer configuration is given at pages 2 and 8 of the specification as filed (emphases added):

> One problem concerns the inadvertent ripping or other damage to the cured filter layers when the wafer is diced into individual chips: **the relatively thin translucent filter layer**, particularly at the photosensors toward either end of the chip, **can be torn by the action of a saw blade.** If the translucent color filter is torn in a manner that even a very small portion (as little as 1%) of the area of one photosite is exposed to unfiltered white light, this extra light thus introduced to the photosite will have an appreciable effect on resulting image quality.
> * * *
> [With the present invention, w]hen a wafer is diced, such as along a groove 70, the fact that each filter layer 74 is disposed over and supported by clear [planar] layer 72, which itself takes up most of the void formed by the groove 70, **the filter layer 74 exhibits very little damage or tearing**, especially in the portions thereof around any photosites 14.

In short, by planarizing (with the planar layer) not only the bulk of a main surface of a chip, but also planarizing each chip even up to a relatively deep groove which defines the edge of a chip, damage to a filter layer during a dicing process is avoided.

Turning to the cited art, the primary reference, Hosier (which of course shares inventors with the present application) discloses a basic end-photosite structure for a photosensitive imaging chip. The secondary reference, Lin, generally teaches planarizing a main surface of the photosensor chip, such as with acrylic or spun-on glass. However, what is not taught in either reference is the idea of planarizing the chip all the way to a groove at an ***dge*** of the chip.

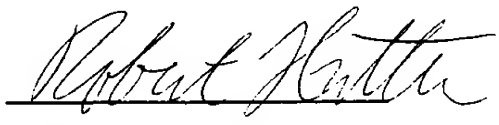
The entire discussion of Lin, with regard to planarization, is directed to maximum light transmission to each photosensor: see, for instance, column 1, lines 31-42. There is no teaching in Lin of the desirability of planarizing at an *edge* of a chip, or at any portion of a chip which is not intended to receive light. A person of skill in the art reading Lin would have no suggestion to combine the general planarization teaching of Lin with Hosier or any other reference to yield the independent claims, each of which recites the planar layer extending over a groove portion at the edge of a chip.

In summary, each independent claim recites a planarization over a **groove** which defines an **edge** of a chip, either within a wafer or after the chips are diced and installed in a larger apparatus. The edge planarization avoids ripping of light-transmissive layers during the dicing process. This edge planarization is not taught or suggested in the prior art.

For this reason, all of the independent claims, and pending claims dependent therefrom, are in condition for allowance.

It is respectfully submitted that the present set of claims are patentably distinct over the cited references. In the event the Examiner considers personal contact advantageous to the disposition of this case, he is hereby requested to call the undersigned attorney at (585) 423-3811, Rochester, NY.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE:

Claims 4 and 5 have been cancelled.

37. (Amended) The method of **claim [30] 31**, further comprising the step of providing in the chip area a ridge defined on the main surface between the photosite and the groove.